EE/CPRE/SE 4920 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 1

8/26/2024 - 9/5/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

Coming back into the semester, we've been able to come back refreshed and ready to work on the project. Progress has been made on the ADC and Priority encoder. The ADC layout is in progress and the priority encoder is at the gate level simulation step however there are some issues with getting it working. The SoC and control signals have also had progress mainly in documenting GPIO ports, pins, and header files for the SoC. There are some issues with the ReRAM layout, which were resolved in the middle of the week; the only steps left are extracting parasitics and running the layout through the MPW precheck.

Past Week Accomplishments:

- Single ReRAM cell has been laid out in magic and is waiting to go through precheck and parasitics simulations.
- Progress on the SoC and GPIO integration.
    - Documented header files, pin presets, and pin bitmasks
    - Learned about process for testing SoC code
        - Code will be written in C and test bench in verilog. Digital hardening process will be followed.
- ADC Schematic Completed

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Started verifying ReRam model in layout	5	66
Gage Moorman	Finished Comparator and ADC schematics	6	66
Nathan Cook	Have documentation made for SoC and did research on header files for the C libraries made for the SoC	7	64
Jason Xie	Finished hardening priority encoder on Openlane. Working to import encoder into Magic and Xschem for post-synthesis testing.	6	64

Pending Issues:

- Gate level simulation for digital hardening is having issues
    - Having some issues correctly flattening and importing spice files into Xschem
- Single cell ReRam
- Having difficulty using ngspice and xschem analysis tools effectively

Plans for the coming week:

- Gage Moorman
    - Finish Comparator and ADC layout and Hardening
    - Build upon analog documentation
- Konnor Kivimagi
    - Finish verifying precheck and parasitics on 1T1R ReRam cell
    - Design and create layouts for larger ReRam arrays
- Nathan Cook
    - Write C test code for GPIO interactions to get familiar with them
    - Work on documentation for the SoC
- Jason Xie
    - Troubleshoot issues importing spice file generated by Openlane into Xschem
    - Assist in writing C test code for control and GPIO

Summary of Advisor Meeting:

We went over where we left off last semester and our current progress. We also went over our teams' strengths and weaknesses from 491. We discussed our timeline, what goals we want to achieve and if the full goal became unrealizable, what the industry panel will look like as well as the 492 timeline.